

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,918,072 B2
DATED : July 12, 2005
INVENTOR(S) : Timothy B. Cowles et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page.

Item [56], **References Cited**, OTHER PUBLICATIONS,

"Micron Technology, Inc.; "Synchronous DRAM" Data Sheets; 128Mb: x32 SDRAM: x32 DRAM, 128MbSDRAMx32, p65—Rev. Sep. 2000, pp. 1-52." should read
-- Micron Technology, Inc.; "Synchronous DRAM" Data Sheets; 128Mb: x32 SDRAM, 128Mb: x32 DRAM, 128MbSDRAMx32, p65 - Rev. Sep. 2000, pp. 1-52. --.

Column 1.

Line 55, "256 chip" should read -- 256 chips --;

Column 13.

Line 2, "address" should read -- addresses --;

Column 14.

Line 39, "illustrates" should read -- illustrate --;

Column 21.

Line 18, "redundant,planes" should read -- redundant planes --; and

Column 22.

Line 31, "scoring" should read -- storing --.

Signed and Sealed this

Twenty-eighth Day of February, 2006



JON W. DUDAS

Director of the United States Patent and Trademark Office